

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Richard K. Williams and Wayne Grabowski

Assignee:

Advanced Analogic Technologies, Inc.

Title:

TRENCH TRANSISTOR WITH CHAINED IMPLANTED BODY

Serial No.:

10/767,030

Filing Date:

January 28, 2004

Examiner:

Belur V. Keshavan

Group Art Unit:

2825

Docket No.:

M7207US4D

San Jose, California

COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, VA 22313-1450

DECLARATION OF PRIOR INVENTION PURSUANT TO 37 C.F.R. § 1.131

I, Richard K. Williams, hereby declare that:

- I and Wayne Grabowski are the inventors of the subject matter claimed in U.S. Pat.
 App. No. 10/767,030 and made that invention before March 31, 1999, while working in
 California;
- 2. Attached as proof of reduction to practice prior to March 31, 1999 or alternatively of conception of the invention prior to March 31, 1999 coupled with due diligence from prior to said date to constructive reduction to practice by the filing on April 22, 1999 of U.S. Pat. App. No. 09/296,959 (herein after the Parent Application) is a copy of a letter dated January 29, 1999, from David E. Steuber, the patent attorney that filed the Parent Application;
 - 3. I received the letter shortly after January 29, 1999; and

THE PATENT LAW OFFICES
OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

PH: (408) 927-6700 PX: (408) 927-6701 4. The Figs. 24A to 24Q referred to in the attached latter were originally prepared by me, were substantially identical to Figs. 24A to 24Q as filed in the Parent Application, and illustrate aspects of the invention now claimed in U.S. Pat. App. No. 10/767,030.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Richard K. Williams

Date

THE PATENT LAW OFFICES
OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

PH: (408) 927-6700 FX: (408) 927-6701



ERVEN, MORRILL, MACPHERSON, FRANKLIN & FRIEL LLP

25 METRO DRIVE, SUITE 700

SAN JOSE, CALIFORNIA 95110 (408) 453-9200

FACSIMILE: (408) 453-7979

January 29, 1999

Mr. Richard K. Williams 10292 Norwich Avenue Cupertino, CA 95014

Re: U.S. Patent Application entitled: "A Super-Self-Aligned Trench-Gate DMOS With

Reduced On-Resistance"

Inventor(s):

Williams, Richard K.; Grabowski, Wayne

Serial No.:

Our Reference:

M-7207 US

Dear Richard:

Enclosed is a first draft of this application. I have proofread the text up to the point where the description of the process sequence begins (Figs. 24A-24Q), but I was unable to complete the proofreading in time to give this to you today. Also, the equations were scrambled in the transition from your program to ours, and we will have them corrected in the next draft.

After you have reviewed this draft, please give me a call so that I can get your comments.

Sincerely yours,

David E. Steuber

DES/mep Enclosure

Enclosure

489091 v1